GOVERNMENT OF INDIA
ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA

STARRED QUESTION NO:101
ANSWERED ON:23.11.2016
FAB Manufacturing Facility
Chudasama Shri Rajeshbhai Naranbhai

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

Will the Minister of Electronics and Information Technology be pleased to state:
(a) the details of assistance, financial and otherwise, provided or proposed for setting up of Semi-Conductor Wafer Fabrication (FAB) units;

(b) the progress made for setting up of Semi-Conductor Wafer Fabrication (FAB) manufacturing facilities in the country;

(c) whether the Government is considering to set up such FAB facilities in various States including Gujarat, if so, the details thereof and the action taken in this regard; and

(d) the locations identified for setting up of FAB manufacturing facilities in the country and the criteria adopted for the same?

Answer

(a) to (d): A statement is laid on the Table of the House.

STATEMENT REFERRED TO IN REPLY TO LOK SABHA STARRED QUESTION NO. *101 FOR 23.11.2016 REGARDING FAB MANUFACTURING FACILITY
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(a) to (d): The Cabinet, in its decision dated 20.04.2011 had set up an Empowered Committee (EC) with the mandate, inter alia, to identify technology and potential investors for setting up Semiconductor Wafer Fabrication (FAB) manufacturing facilities in the country, and to recommend nature and quantum of Government support.

2. The Empowered Committee adopted a proposal-based initiative for inviting Expression of Interest (EoI) for setting up of FAB facilities with the aim of attracting investments in a complex and financially challenging hi-tech manufacturing sector. In response to the EoI, proposals were received from two business consortia, one led by M/s. Jaiprakash Associates Limited (with IBM, USA and Tower Semiconductor Limited, Israel as partners with proposed location as Yamuna Expressway, Uttar Pradesh) and the other led by M/s. HSMC Technologies India Pvt. Ltd. (with ST Microelectronics and Silterra Malaysia Sdn. Bhd. as partners with proposed location as Prantij, Gujarat).

3. Empowered Committee, after detailed appraisal of the two proposals submitted its recommendations with respect to their strategic fit to the national requirements, implementation capabilities of the consortia, technologies proposed and the minimum quantum of incentives required to make the FAB projects viable.

4. Letters of Intent (LoI) dated 19.03.2014 were issued to the two consortia for setting up of Semiconductor FAB facilities in India. For Demonstration of Commitment, both Consortia were required to submit certain documents. The following main incentives were extended:

a) 25% subsidy on capital expenditure and tax reimbursement as admissible under Modified Special Incentive Package Scheme (M-SIPS) Policy
b) Exemption of Basic Customs Duty (BCD) for non-covered capital items
c) Deduction on expenditure on R&D as admissible under Section 35(2AB) of the Income Tax (IT) Act
d) Investment linked deduction under Section 35AD of the IT Act
e) Interest free loan of approx. Rs.5,124/- crores each (Exact to be calculated on appraisal of Detailed Project Reports), which shall be capped at 20% of the capital expenditure (as admissible under M-SIPS)

5. Subsequently, both M/s. HSMC Technologies India Pvt. Ltd. and M/s. Jaiprakash Associates Ltd. had sought extension of time on multiple occasions for submission of deficiencies in Detailed Project Reports and other documents required for demonstration of commitment, which was provided to them by the EC.

6. While the consortium led by M/s. Jaiprakash Associates Ltd. has thereafter withdrawn from the project in March 2016, the consortium led by M/s. HSMC Technologies India Pvt. Ltd. has been putting in efforts to attract equity and debt funding for setting up the Semiconductor FAB project. Considering the importance of project to the country from both strategic and economic point of view; the project being highly capital intensive and technologically challenging as well as essential for fostering the electronics design and

manufacturing ecosystem in the country, EC was of the view in its meeting held on 17.08.2016 that it would be worthwhile to provide the consortium led by M/s. HSMC Technologies India Pvt. Ltd. some more time to make efforts to submit all the documents required for demonstration of commitment, as per the Letter of Intent (LoI) dated 19.03.2014. The EC recommended that the progress made by the consortium be closely monitored. Subsequently, based on the progress made and request of the consortium led by M/s. HSMC Technologies India Pvt. Ltd., the EC shall take a view on providing further extension for submission of all the documents for demonstration of commitment, as per the terms and conditions of the LoI.

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