GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
**LOK SABHA**
**UNSTARRED QUESTION NO. 3322**
TO BE ANSWERED ON: 09.08.2023

## BUILDING SEMICONDUCTOR ECOSYSTEM

**3322. SHRI PRADYUT BORDOLOI:**

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) the details of the proposed Rs. 76,000 crore subsidies for building India's semiconductor ecosystem, including fund allocation to areas like semiconductor components manufacturing, display panels, specialized components and packaging/testing ICs;
(b) the steps and initiatives taken by the Government to support and incentivize the growth of export-oriented chip design companies (fabless companies) in India, considering the potential for building a world-class export industry in semiconductor design and manufacturing;
(c) the details of the Government's plan to promote and encourage research and development in semiconductor technology particularly in the area of designing state-of-the-art product innovations;
(d) whether the Government intends to support and collaborate with academic institutions and private research organisations for this purpose; and
(e) if so, the details thereof and if not, the reasons therefor?

**ANSWER**

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI RAJEEV CHANDRASEKHAR)

(a) and (b): Government is focused on its objective of catalysing overall semiconductor ecosystem to further expand India's already rapidly expanding electronics manufacturing and innovation ecosystem. Government has approved the Semicon India programme with a total outlay of INR 76,000 crore for the development of semiconductor and display manufacturing ecosystem in the country. The total fiscal outlay of Rs 76,000 crore is fungible across different schemes under the programme.The programme aims to provide financial support to companies investing in semiconductors, display manufacturing and design ecosystem. This will serve to pave the way for India's growing presence in the global electronics value chains. Following four schemes have been introduced under the aforesaid programme:

i. '**Modified Scheme for setting up of Semiconductor Fabs in India**' for attracting large investments for setting up semiconductor wafer fabrication facilities in the country to strengthen the electronics manufacturing ecosystem and help establish a trusted value chain. The Scheme extends a fiscal support of 50% of the project cost on *pari-passu* basis for setting up of Silicon CMOS based Semiconductor Fab in India.
ii. '**Modified Scheme for setting up of Display Fabs in India**' for attracting large investments for manufacturing TFT LCD or AMOLED based display panels in the country to strengthen the electronics manufacturing ecosystem. Scheme extends fiscal support of 50% of Project Cost on *pari-passu* basis for setting up of Display Fabs in India.
iii. '**Modified Scheme for setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab / Discrete Semiconductors Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / OSAT facilities in India'** extends a fiscal support of 50% of the Capital Expenditure on Pari-passu basis for setting up of Compound Semiconductors / Silicon Photonics (SiPh) / Sensors

(including MEMS) Fab/ Discrete Semiconductor Fab and Semiconductor ATMP / OSAT facilities in India.

iv. **'Semicon India Future Design: Design Linked Incentive (DLI) Scheme'**offers financial incentives, design infrastructure support across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design. The scheme provides "Product Design Linked Incentive" of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application and "Deployment Linked Incentive" of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application.

In addition to the above schemes, Government has also approved modernisation of Semi-Conductor Laboratory, Mohali as a brownfield Fab.

(c), (d) and (e): Government has initiated 'Semicon India Future Skill: Chip to Startup (C2S) Programme' to promote industry-led R&D, translational research and strengthening Industry Academia collaboration in addition to the 'Semicon India Future Design: Design Linked Incentive (DLI) Scheme'. Further, a R&D Committee has been constituted comprising of representatives from global semiconductor Industry, Academia and Government to create a roadmap for semiconductor R&D in India.

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